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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/241,994	02/02/1999	RONALD M. HICKLING	TECHCON.001A	9408

7590 07/10/2003

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EXAMINER	
TSE, YOUNG TOI	
ART UNIT	**PAPER NUMBER**
2634	24

DATE MAILED: 07/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/241,994	HICKLING, RONALD M.	
	Examiner	Art Unit	
	YOUNG T. TSE	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-12 and 14-19 have been considered but are moot in view of the new ground(s) of rejection (Reber is now use as a primary reference and De Vries er al. as a secondary reference).

2. Applicant's arguments filed March 11, 2003 have been fully considered but they are not persuasive.

With respect to the declaration of prior invention in the United States to overcome cited patent or publication (37 C.F.R. 1.131), the declaration can not overcome the prior art Reber and De Vries et al. because the invention shown in Fig. 2.3.1 of Exhibit 2 is different than the present invention of the instant application shown in Fig. 4.

In the present invention of Fig. 4, the delta-sigma modulator 64 comprises a commutator circuit including a complementary amplifier 76 and a switch 78; a core delta-sigma modulator including a loop amplifier 80, a loop filter 82, an edge-trigger comparator 84 and a 1-bit digital-to-analog converter 86; and a common clock CLK to control the switch 78 and the edge-trigger comparator 84.

The complementary amplifier 76 receives a digitally modulated RF signal centered about the carrier frequency. At an inverting output, the complementary amplifier 76 produces a voltage that is –G times the voltage at the input to the complementary amplifier 76. The inverting and non-inverting outputs of the complementary amplifier 76 are coupled to two input ports of the switch 78. The control

port of the switch 78 determines which input port is coupled to the output port and is driven by the conversion clock, CLK, such that the output port of the switch 78 is alternately coupled to the inverting and non-inverting outputs of the complementary amplifier 76. The output of the switch 78 is coupled to the input of the core delta-sigma modulator.

However, in Fig. 2.3.1 of the Exhibit 2, the digital I-Q modulator comprises a GaAs integrated circuit and a silicon CMOS integrated circuit.

The GaAs integrated circuit comprises a mixer for mixing a modulated input carrier frequency with a clock input, an amplifier having an inverting and a non-inverting inputs and an output, two analog-to-digital converters, two digital-to-analog converters, a switch for selecting one of the outputs of the two digital-to-analog converters and is controlled by the clock input to output a signal to the non-inverter input of the amplifier, and a time division demultiplexer for providing an IF signal to the silicon CMOS integrated circuit.

The silicon CMOS integrated circuit comprises a 320 tap digital FIR filter receives the IF signal and is controlled by a clock, a data rate reduction circuit, and a quadrature modulator for providing I and Q output signals.

The Exhibit 2 does not fully describe the operation of the block elements of Fig. 2.3.1. Although the Exhibit 2 mentions that the mixer is actually a "chopper" which effectively multiplies the input by a "+1, -1, +1, ..." sequence that is equivalent to negating the gain polarity of the input amplifier on every halt of the clock. In the instant application, the polarity of the commutator signal is obtained by the switch 78 by

alternately selecting the inverting output and the non-inverting output of the complementary amplifier 76 controlled by the clock CLK. In contrast, Exhibit 2 does not teach which circuitry generates the polarity of the commutator signal. In other words, Exhibit 2 does not teach or show the principle invention as show in Fig. 4 and the claimed subject matter of claims 1-12 and 14-19 in the instant application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8, 10-12, and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reber in view of De Vries et al.

Reber (U.S. Patent No. 6,393,070 B1) discloses a digital wireless communication system in Fig. 1 which includes an amplifier (20), a first bandpass filter (5), a first mixer (3), a second bandpass filter (9), an AGC (10), a mixer and sampler (11) including a second mixer (12) and a bit stream analog-to-digital converter stage (13), and a DSP (16).

Fig. 2 shows the detailed embodiment of the mixer and sampler (11). Referring to Fig. 2, the mixer and sampler (11) comprises a mixer or a controllable inverter circuit (12) for inverting the polarity of the input signal (20) or the output signal of the AGC circuit (10), an intermediate frequency (IF) signal from the RF stage, is fed to the first

input (20) of the controllable inverter stage (12) and a square wave signal having a radian frequency is fed to a second input (21) of the inverter stage (12) to provide a converted or non-converter IF signal, see column 3, lines 3-10 and 27-33; a sigma delta modulator (25) for converting the inverted input signal into a series of digital values (26), and a decimation filter (27) for filtering the series of digital values (26) into digital filter values (28) to provide a baseband signal.

With respect to each of the independent claims 1, 7, and 14, the inverter circuit (12) corresponds to the polarity inverting circuit or commutator circuit and the sigma delta modulator (25) corresponds to the delta-sigma modulator.

With respect to claims 2-3, 5-6, 11-12, 15-16, and 18-19, Reber shows the communication device in Fig. 1 wherein the input signal of the inverter circuit (12) is derived from an antenna (3) through the amplifier (2), the first bandpass filter 5, the first mixer (6), the second bandpass filter (9), and the AGC circuit (10). As shown in Fig. 1 and Fig. 2, the communication device (1) and the mixer and sampler circuit (11) are fabricated on a single substrate.

Reber does not explicitly show or suggest that the inverter circuit (12) and the sigma delta modulator (25) are provided by a common clock signal for inverting the polarity of the input signal (20) on every one half clock cycle of the clock signal to produce a commutated waveform before converting the commutated waveform to a series of digital values by the sigma delta modulator (25).

DeVries et al. (U.S. Patent No. 5,736,848) discloses a communication system in Fig. 2 for measuring the energy output from one or more electrical energy sources first

makes an analog power measurement, and converts the resultant output into digital from.

Referring to Fig. 2, the communication system includes at least an analog power measuring system (1) for inverting a polarity of the input signal u[t], an analog to digital converter (2) including a sigma delta modulator (8) and a digital filter (9) for converting the inverted polarity of the input signal into a series of digital values, and a common clock (CL 1) for providing a common clock signal to both the analog power measurement system (1) and the sigma delta modulator (8). See column 3, lines 22-35.

Fig. 1 shows the detailed embodiment of the analog power measurement system (1) of Fig. 2. Referring to Fig. 1, the analog power measurement system (1) includes at least a polarity reverser switch (3) including two switch poles for providing the polarity of the input signal through a magnetic field sensor (5) and an amplifier (7). See column 2, line 28 to column 3, line 21.

Although De Vries et al. does not explicitly show or suggest that the inverted input signal is inverted on every one half clock cycle of the common clock (CK 1). De Vries et al. teaches the polarity reverser (3) consists of a two-polarity commutator in the form of the polarity (3) and whose control input constitutes a clocking input of the analog power measuring system (1) fed the clocking signal (CL 1). The two-pole commutator consists of four on/off switches which are operated by means of two inverters two by two in push-pull action and thus constitute two single-pole commutators which are commutated synchronously. See column 2, lines 54-64.

De Vries et al. also teaches a two-pole output of the analog power measuring system (1)) is connected to a two-pole input of the sigma-delta modulator (8) with a switching input fed the same clocking signal (CL 1) as the clocking input of the arrangement (1). The sigma-delta modulator (8) contains a polarity reverser (PR in block 8 of Fig. 4) which is commuted periodically by means of the clocking signal (CL 1) in synchronism with the polarity reverser (3) of the arrangement (1) in order to realize polarity commutations. As a consequence, the desired signal is twice polarity-reversed synchronously, once the arrangement (1) and once in the sigma-delta modulator (8). See column 3, lines 24-35.

In other words, when the on/off switches which are operated by means of two inverters two by two in push-pull action and are periodically synchronized with each other. The input signal u[t] is inverted on every one quarter clock cycle, half clock cycle, three quarter clock cycle or full clock cycle.

Therefore, it would have been obvious to one or ordinary skill in the art to provide a common clock signal to both the inverter circuit (12) and the sigma delta modulator (25) of Reber's mixer and sampler (11) of the receiver circuit as taught by De Vries in order to convert the polarity of the input signal (20) on every one half clock cycle of the common clock signal to produce a commutated waveform before converting the commutated waveform to a series of digital values by the sigma delta modulator (25).

With respect to claims 4, 8, and 17, De Vries clearly shows that the analog power measuring system (1) includes at least the polarity reverser switch (3), the servo

amplifiers (4), and the amplifier (7) and the analog to digital converter (2) for converting the commutated waveform into a frequency offset baseband.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Reber in view of De Vries et al. and Ichimura et al.

Reber discloses a digital wireless communication system in Fig. 1 which includes an amplifier (20), a first bandpass filter (5), a first mixer (3), a second bandpass filter (9), an AGC (10), a mixer and sampler (11) which including a second mixer (12) and a bit stream analog-to-digital converter stage (13), and a DSP (16).

Fig. 2 shows the detailed embodiment of the mixer and sampler (11). Referring to Fig. 2, the mixer and sampler (11) comprises a mixer or a controllable inverter circuit (12) for inverting the polarity of the input signal (20) or the output signal of the AGC circuit (10), an intermediate signal (IF) from the RF stage, is fed to the first input (20) of the controllable inverter stage (12) and a square wave signal having a radian frequency is fed to a second input (21) of the inverter stage (12) to provide a converted or non-converter IF signal, see column 3, lines 3-10 and 27-33; a sigma delta modulator (25) for converting the inverted input signal into a series of digital values (26), and a decimation filter for filtering the series of digital values into digital filter values (28) to provide a baseband signal.

DeVries et al. (U.S. Patent No. 5,736,848) discloses a communication system in Fig. 2 for measuring the energy output from one or more electrical energy sources first makes an analog power measurement, and converts the resultant output into digital from.

Referring to Fig. 2, the communication system includes at least an analog power measuring system (1) for inverting a polarity of the input signal u[t], an analog to digital converter (2) including a sigma delta modulator (8) and a digital filter (9) for converting the inverted polarity of the input signal into a series of digital values, and a common clock (CL 1) for providing a common clock signal to both the analog power measurement system (1) and the sigma delta modulator (8). See column 3, lines 22-35.

Fig. 1 shows the detailed embodiment of the analog power measurement system (1) of Fig. 2. Referring to Fig. 1, the analog power measurement system (1) includes at least a polarity reverser switch (3) including two switch poles for providing the polarity of the input signal through a magnetic field sensor (5) and an amplifier (7). See column 2, line 28 to column 3, line 21.

Both Reber and DeVries et al. fail to show the detailed embodiment of the sigma-delta modulators (25) and (8) as recited in the dependent claim 9 and the independent claim 28.

Ichimura et al. (U.S. Patent No. 5,835,042) discloses the detailed embodiment of a sigma-delta modulator (3) in Fig. 3 which includes an adder (11) for adding an input signal (2) from a feedback signal, an integrator (12), a comparator (13), a sample delay (14), and a 1 bit D/A converter (15) for providing the feedback signal to the adder (11).

With respect to claim 9, the integrator (12) may consider as the loop amplifier and the continuous time loop filter; the comparator (13) may consider as the edge-triggered comparator; and the 1 bit D/A converter (15) may consider as the one-bit digital to analog comparator.

Applicant note although Ichimura et al. does not mention that the integrator (12) is consisted of a loop amplifier and a loop filter. It is well known to a person skill in the art that a loop amplifier and a loop filter act as an integrator. Also see page 11, lines 8-9 of the instant application.

Therefore, it would be been obvious to one of ordinary skill in the art to use a common clock signal to both the inverter circuit (12) and the sigma delta modulator (25) of Reber's mixer and sampler (11) of the receiver circuit as taught by De Vries in order to convert the polarity of the input signal (20) on every one half clock cycle of the common clock signal to produce a commutated waveform before converting the commutated waveform to a series of digital values by the sigma delta modulator (25) include a loop amplifier, a loop filter, a comparator, and a one-bit D/A converter in the sigma-delta modulator (25) of Reber's wireless receiver as taught by Ichimura et al. in order to overcome the problem of long ladder carry propagation delays or its simplicity and its robustness against circuit imperfections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Young Tse** whose telephone number is **(703) 305-4736**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Stephen Chin**, can be reached at **(703) 305-4714**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
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or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Or:

(703) 872-9315 (for amendments after final rejection only, please mark "EXPEDITED PROCEDURE")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Young T. Tse
Primary Examiner
7/6/03